Amendment to the Drawings

The attached sheet of drawings includes changes to Figure 4. This sheet, which includes Figure 4, replaces the original sheet that includes Figure 4.

Attachment: 1 Replacement Sheet

REMARKS

In the Office Action, the Examiner objected to claims 3, 7, and 17 for informalities. The Examiner also rejected claims 1 and 2 under 35 U.S.C. §102(b) as being unpatentable over United States Patent 5,357,604 issued to San, et al. ("San"). The Examiner also rejected claim 3 under 35 U.S.C. §103(a) as being unpatentable over San in view of United States Patent 6,353,874 issued to Morein, et al. ("Morein"). The Examiner also reject claims 4-6, 10, and 11 under 35 U.S.C. §103(a) as being unpatentable over San in view of United States Patent 6,809,732 issued to Zatz, et al. ("Zatz"). The Examiner also rejected claim 7 under 35 U.S.C. §103(a) as being unpatentable over San and Zatz in view of Morein. The Examiner also rejected claims 8, 9, and 12 under 35 U.S.C. §103(a) as being unpatentable over San and Zatz in view of United States Patent 6,088,701 issued to Whaley, et al. ("Whaley"). The Examiner also rejected claim 13 under 35 U.S.C. §103(a) as being unpatentable over San and Zatz in view of United States Patent 4,876,651 issued to Dawson, et al. ("Dawson"). The Examiner also rejected claims 14-16, and 20 under 35 U.S.C. §102(b) as being unpatentable over United States Patent 6,016,151 issued to Lin, et al. ("Lin"). The Examiner also rejected claims 17 and 19 under 35 U.S.C. §103(a) as being unpatentable over Lin in view of Zatz. The Examiner also rejected claim 18 under 35 U.S.C. §103(a) as being unpatentable over Lin and Zatz in view of Whaley.

In this Amendment, Applicants have amended the claims 1, 3, 4, 5, 7 and 17. Applicants have not added or canceled any claim. Accordingly, claims 1-20 will be pending after entry of this Amendment.

I. Amendments to the Specification

Applicants have amended the Specification to correct certain typographical errors. The first two corrections change the reference label for the image processing routine from 130 to 120. These changes are supported both by the reset of the text in the amended paragraphs and by the labels in Figure 1.

The last correction changes "as described in relation to **Figure 5**" to "as described in relation to **Figure 2**". The discussion in the text is clearly about **Figure 3** in relation to **Figure 2**. These amendments do not add any new matter since the corrections to the typographical errors are supported both by the rest of the text and by the corresponding diagrams. Applicants respectfully request that the Examiner approve the amendments.

II. Amendments to the Drawings

Applicants have amended Figure 4 by submitting the attached sheet of drawing. Changes to the drawing are supported by the text describing the figures. Specifically, the reference label for the frame number axis is changed from 440 to 450 and the reference label for the effect tree is specified to be 440. Applicants respectfully request that the Examiner approve the enclosed drawings.

III. Objection to Claims 3, 7 and 17

In the Office Action, the Examiner objected to claims 3, 7, and 17 for informalities. In this Amendment, Applicants have amended claims 3, 7, and 17 to correct the informalities. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the objections to claims 3, 7, and 17.

IV. Rejection of Claims 1-3

In the Office Action, the Examiner rejected claims 1-2 under §102(b) as being unpatentable over San. The Examiner also rejected claim 3 as being unpatentable over San in view of Morein. Claims 2 and 3 are dependent on claim 1.

Claim 1 recites a method of executing a set of two or more image processing routines on a processor using a cache. Each routine in the set of routines processes at least a source. Each source is a frame of video data. The method determines a size of a band of the sources of the set of routines. Each source includes two or more bands where the size of the band is related to a size of the cache. The method executes the set of routines in two or more passes, where a pass of the set of routines includes each routine in the set of routines processing a single band of its source retrieved from the cache to produce output data stored to the cache.

Applicants respectfully submit that San does not make claim 1 unpatentable for at least the following reasons. *First*, San does not disclose processing the source retrieved from the cache where the source is a frame of video data. In fact, San teaches away from video data stored in a cache since San specifies that the cache is used to store the program for a graphics coprocessor. Specifically, San in column 3, lines 22-27 specifies: "[t]he graphics coprocessor of the present invention also includes a unique 'CACHE' instruction and a cache memory and controller mechanism which permit program instructions stored in the program ROM to be executed at high speed by the graphics coprocessor from cache RAM".

Also, in the Office Action, the Examiner has cited column 16, lines 16 to 30 of San and has specified: "cache RAM 94 is a 512-byte instruction cache ... any program loop that can fit into the 512 bytes cache size can run at full speed, one cycle for both fetch and execute ..."

[Emphasis added by Applicants]. Applicants respectfully submit that the portions of the Examiner quote underlined by the Applicants clearly show that the cache in San is used to execute program code. Therefore, San does not process a source retrieved from the cache where the source is a frame of video data.

Second, San does not specify determining a size of a band of the sources where the size of the band is related to a size of the cache. In the Office Action, the examiner lumped several limitations of claim 1 together and has specified the following to reject them: "cache RAM 94 is a 512-byte instruction cache … any program loop that can fit into the 512 bytes cache size can run at full speed, one cycle for both fetch and execute … running a loop inside the cache 94 using the PLOT instruction to write the pixel to RAM 6, 8, Col. 16, lines 16-30; Mario chip can execute programs which implement algorithms to manipulate the background and foreground of sprites or moving objects, Col. 19, lines 47-50." [Emphasis added by Applicants] Applicants respectfully submit that neither in the cited paragraphs not anywhere else, San specifies determining a size of a band of the sources where the size of the band is related to a size of the cache. In fact, San does not specify any method of using banded sources in its video chip.

Third, San does not specify a method of executing a set of routines in two or more passes, where in each pass, each routine processes a band of its source retrieved from the cache to produce output data stored to the cache. Specifically, the Examiner has used the quote specified in the *second* argument above to also reject this limitation. Applicants respectfully submit that neither in the paragraphs cited by the examiner nor anywhere else San specifies a routine that in each pass, processes a band of its source retrieved from the cache to produce output data stored to the cache.

Fourth, San specifies that the programmer must decide how best to utilize the program cache that "has a small size compared to the size of the average program" [Emphasis added]. *See* San, column 16, lines 16-24. Thus, San specifies a system used by a programmer to allocate cache for program execution rather than a method that determines the size of a band of a frame of video data.

Applicants have Amended claim 1 to clarify the use of the cache. The Amendment is made for reasons of clarity and not for reasons of patentability. Applicant does not surrender any equivalents of the amended elements.

In view of the foregoing remarks, Applicants respectfully submit that San does not render claim 1 unpatentable. As claims 2 and 3 are dependent on claim 1, Applicants respectfully submit that claims 2 and 3 are patentable over San for at least the reasons that were discussed above for claim 1. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the §102(b) rejection of claims 1-3.

V. Rejection of Claims 4-9

In the Office Action, the Examiner rejected claims 4-6 under §103(a) as being unpatentable over San in view of Zatz. The Examiner also rejected claim 7 as being unpatentable over San and Zatz in view of Morein. The Examiner also rejected claims 8 and 9 under 35 U.S.C. §103(a) as being unpatentable over San and Zatz in view of Whaley.

Claims 5-9 are directly or indirectly dependent on independent claim 4. Claim 4 recites a method of processing a group of image processing routines on a processor using a cache. Each routine in the group of routines processes at least a source. Each source is a frame of video data. The method determines an initial list of routine identifiers that includes a group of routine identifiers positioned in a specific order. The group of routine identifiers identifies the group of image processing routines. Each routine identifier in the group of routine identifiers identifies a corresponding routine in the group of routines. The method groups two or more routine identifiers of the group of routine identifiers into a set of routine identifiers that identify a set of routines. The method modifies the initial list of routine identifiers to indicate the grouping of the two or more routine identifiers to produce a modified list of routine identifiers. The method also determines a size of a band of the sources of the set of routines, each source includes two or more bands where the size of the band is related to the size of the cache.

Applicants respectfully submit that San, Zatz, or their combination do not disclose, teach or even suggest the method of claim 4 for at least the following reasons. *First*, Applicants respectfully submit that the cited references or their combination do not specify a method that determines an initial list of routine identifiers. In the Office Action, the Examiner cited Column 21, lines 66-67 and column 23, lines 6-14 of San. Applicants respectfully submit that the cited paragraphs refer to Mario chip's instructions set and does not determine an initial set of routine identifiers. Specifically, the cited paragraphs respectively specify: "[a] detailed listing of the instruction set id also included." and "[i]n the ALT 1 mode identified above, an ADD instruction will be interpreted as an ADD WITH CARRY and a SUBTRACT instruction will be interpreted as SUBTRACT WITH CARRY. ...". Applicants respectfully submit that neither in the cited paragraphs nor anywhere else, do San or Zatz specifies an initial list of routine identifiers.

Second, Applicants respectfully submit that since the cited references doe not specify routine identifiers, the cited references also do not specify positioning the routine identifiers in a specific order. For the same reason, the cited references also do not specify that routine identifiers identify image processing routines.

Third, Applicants respectfully submit that San, Zatz, or their combination does not specify a method for determining a size of a band of the sources where the size of the band is related to a size of the cache. In the Office Action, the examiner cited column 16, lines 16-30 and column 19, lines 37-50 of San for specifying such a method. Applicants respectfully submit that the cited paragraphs do not specify such a method. Specifically, the cited column 16, lines 16-30 of San specify:

> Cache RAM 94 may be a 512-byte instruction cache. This is a relatively small size compared to the size of the average program, so the programmer must decide how best to utilize the cache memory 94. Any program loop that can fit into the 512 bytes cache size can run at full speed, one cycle for both fetch and execute. Because of the split busses, both ROM and RAM can be simultaneously accessed while executing code from internal cache 94.
>
> The cache RAM 94 may be advantageously used to rotate a sprite by running a loop inside the cache 94 that would read the color of each pixel from ROM 10 while it is performing the rotation and scaling calculations, while it is using the PLOT instruction (to be described below) to write the pixel to RAM 6, 8.

Also the cited column 19, lines 37-50 of San specify:

> When the Super NES has need to use the Mario chip processing power to perform either graphics operations or mathematical calculations, the Super NES stores the appropriate data it desires the Mario chip to process in the cartridge RAM (or in predetermined Mario registers) and loads the Mario chip program counter with the address of the Mario program to be executed. The data to be processed by the Mario chip may be predetermined X, Y coordinate data of objects which must be rotated and enlarged or reduced. The Mario chip can execute programs which implement algorithms to manipulate the background and foreground of sprites or moving objects of varying number. The use of the Mario chip speed enhancing hardware and software results in high speed performance of such operations.

Applicants respectfully submit that neither in the cited paragraphs not anywhere else, San or Zatz specify determining a size of a band of the sources where the size of the band is related to a size of the cache.

Fourth, Applicants respectfully submit that the cited references or their combination do not specify a method that groups two or more routine identifiers of a group of routine identifiers into a set of routine identifiers that identify a set of routines. In the Office Action, the Examiner correctly indicated that San does not specify such a method. The Examiner, however, quoted the followings from column 9, lines 2-6 of Zatz for specifying such a method: "if two program instructions each specify a simple texture operation, codewords derived from each of these program instructions can be combined into one codeword representation for execution". Furthermore, Zatz defines a codeword as "the native control format comprises a collection of codewords, where each codeword specifies an operation, such as addition or multiplication, and optionally other configuration information such as operand and result precision, constants, condition codes, source and destination registers, and the like." *See*, Zatz column 8, lines 29-34. The codewords are, therefore, not routine identifiers. Applicants respectfully submit that the cited paragraph specifies combining program instructions into one codeword and does not specify a method that groups two or more routine identifiers of a group of routine identifiers into a set of routine identifiers that identify a set of routines.

Fifth, Applicants respectfully submit that the cited references or their combination do not specify a method that modifies the initial list of routine identifiers to indicate the grouping of the two or more routine identifiers to produce a modified list of routine identifiers. In the Office

Action, the Examiner correctly indicated that San does not specify such a method. The Examiner, however, quoted the following from column 16, lines 42-53 of Zatz for specifying such a method: "multiple separate sets of data can be processed, dataflow tokens output advantageously serve to signal a computation unit to reconfigure itself with codewords from the dataflow token". Applicants respectfully submit that the cited paragraph specifies reconfiguration of a computation unit and does not specify modifying a list of routine identifiers to indicate the groupings of the two or more routine identifiers as specified in claim 4.

In view of the foregoing remarks, Applicants respectfully submit that San, Zatz, or their combination does not disclose, teach, or even suggest the method of claim 4. As claims 5-9 are directly or indirectly dependent on claim 4, Applicants respectfully submit that claims 5-9 are patentable for at least the reasons that were discussed above for claim 4. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the §103(a) rejection of claims 4-9.

VI. Rejection of Claims 10-13

In the Office Action, the Examiner rejected claims 10 and 11 under §103(a) as being unpatentable over San in view of Zatz. The Examiner also rejected claim 12 under 35 U.S.C. §103(a) as being unpatentable over San and Zatz in view of Whaley. The Examiner also rejected claim 13 under 35 U.S.C. §103(a) as being unpatentable over San and Zatz in view of Dawson.

Claims 11-13 are directly or indirectly dependent on independent claim 10. Claim 10 recites a method of processing a group of routines. The method determines an initial list of routine identifiers that include a group of routine identifiers identifying the group of routines. Each routine identifier in the group of routine identifiers identifies a corresponding routine in the group of routines. The method identifies a set of two or more routine identifiers in the initial list of routine identifiers that identify a set of two or more routines that are combinable into a single routine. The single routine is capable of performing each routine in the set of routines. The method determines a single routine identifier that identifies the single routine.

Applicants respectfully submit that San, Zatz, or their combination do not disclose, teach or even suggest the method of claim 10 for at least the following reasons. *First*, Applicants respectfully submit that the cited references or their combination do not specify a method that determines an initial list of routine identifiers. In the Office Action, the Examiner cited Column 21, lines 66-67 and column 23, lines 6-14 of San. Applicants respectfully submit that the cited paragraphs refer to Mario chip's instructions set and does not determine an initial set of routine identifiers. Specifically, the cited paragraphs respectively specify: "[a] detailed listing of the instruction set id also included." and "[i]n the ALT 1 mode identified above, an ADD instruction will be interpreted as an ADD WITH CARRY and a SUBTRACT instruction will be interpreted as SUBTRACT WITH CARRY. ...". Applicants respectfully submit that neither in the cited paragraphs nor anywhere else, do San or Zatz specifies an initial list of routine identifiers.

Second, Applicants respectfully submit the San, Zatz, or their combination do not disclose, teach, or even suggest a method that identifies a set of two or more routine identifiers that are combinable into a single routine, the single routine being capable of performing each routine in the set of routines. In the Office Action, the Examiner correctly indicated that San does not specify such a method. The Examiner, however, cited column 8, line 62 to column 9, line 6 of Zatz for specifying such a method. The Examiner also referred to reasons given in the rejection of claim 4. Applicants respectfully submit that the cited paragraph specifies:

> Other embodiments implement optimizations that generate more efficient native control information representations of received control information. In an embodiment, Programmable Shader 153 determines whether codewords that describe the operations represented by two or more program instructions can be combined into fewer codewords. For instance, Shader Core 230 is capable of executing two simple texture operations at one time. Thus, if two program instructions each specify a simple texture operation, codewords derived from each of these program instructions can be combined into one codeword representation for execution on Shader Core 230.

Applicants respectfully submit that the cited paragraph specifies combining codewords and not routine identifier that are combinable into a single routine, the single routine being capable of performing each routine in the set of routines. Specifically, Zatz defines a codeword as "the native control format comprises a collection of codewords, where each codeword specifies an operation, such as addition or multiplication, and optionally other configuration information such as operand and result precision, constants, condition codes, source and destination registers, and the like." See, Zatz column 8, lines 29-34.

Third, Applicants respectfully submit the piecemeal, hindsight combination of the cited references do not disclose, teach or even suggest such a method. For instance, the combination does not disclose, teach or even suggest:

- Determining an initial list of routine identifiers comprised of a group of routine identifiers identifying the routines, or
- Identifying a set of two or more routine identifiers in the initial list of routine identifiers that identify a set of two or more routines that are combinable into a single routine.

Accordingly, Applicants respectfully submit that the cited references do not render claim 10 unpatentable. As claims 11-13 are directly or indirectly dependent on claim 10, Applicants respectfully submit that claims 11-13 are patentable over the cited references for at least the reasons that were discussed above for claim 10. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the §103(a) rejection of claims 10-13.

VII. Rejection of Claims 14- 20

In the Office Action, the Examiner rejected claims 14-16, and 20 under §102(b) as being unpatentable over Lin. The Examiner also rejected claim 17 and 19 as being unpatentable over Lin in view of Zatz. The Examiner also rejected claim 18 as being unpatentable over Lin and Zatz in view of Whaley.

Claim 15-20 are directly or indirectly dependent on independent claim 14. Claim 14 recites a method of executing a group of routines that are able to be executed on a first processor. The method determines an initial list of routine identifiers that includes a group of routine identifiers identifying the group of routines. Each routine identifier in the group of routine identifiers identifies a corresponding routine in the set of routines. The method identifies a routine identifier in the initial list of routine identifiers as a sendable routine identifier that identifies a sendable routine able to be processed by a second processor.

Applicants respectfully submit that Lin does not anticipate the method of claim 14 for at least the following reasons. Applicants respectfully submit that Lin does not specify a method that identifies a routine identifier in the initial list of routine identifiers as a sendable routine identifier that identifies a sendable routine to be processed by a second processor. In the Office Action, the Examiner cited column 7, line 51 to column 8, line 6 of Lin for specifying such a method. Specifically the Examiner specified: "Lin describes that routines having to do with texture gradients and the starting vertex and its texture attributes are sent from the host CPU to graphics accelerator (40). These routines are identified by texture attributes such as rhw (Col. 7, line 51-Col. 8, line 6)." *See* the Office Action, page 4, item 9. Applicants respectfully submit that the quoted paragraph specifies sending attributes to a graphic accelerator and not identifying routine identifiers able to be processed by a second processor. Specifically, the paragraph cited by the Examiner also specifies: "[t]hese texture gradients are then used by graphics accelerator 40 to perform texture triangle-walking step 32 and texture interpolation and lookup step 28. Therefore, Lin's texture attributes (parameters) are passed to the graphics accelerator to parameterize the texture triangle-walking step 32 and the texture interpolation and lookup step 28 and not to identify these routine identifiers that are able to be sent to and processed by a second processor.

Accordingly, Applicants respectfully submit that Lin does not render claim 14 unpatentable. As claims 15-20 are directly or indirectly dependent on claim 14, Applicants respectfully submit that claims 15-20 are patentable over the cited references for at least the reasons that were discussed above for claim 14. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the §102(b) rejection of claims 14-20.

CONCLUSION

In view of the foregoing, it is submitted that all the claims, namely claims 1-20, are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

STATTLER, JOHANSEN & ADELI LLP

Dated: 4/12/06

Ali Makoui
Reg. No. 45,536

Stattler Johansen & Adeli LLP
1875 Century Park East, Suite 1360
Century City, CA 90067-2514
Phone: (310)785-0140 x302
Fax: (310)785-9558

ATTACHMENT